62. (Amended) A data processor performing data processing based on an 8-bit instruction, comprising:

a plurality of registers;

a decoding unit decoding an 8-bit instruction, the instruction independently designating:

one of a plurality of operations including transfer and calculation;

one of the plurality of registers as a source operand, and

one of the plurality of registers as a destination operand;

wherein at least one of the source operand register and the destination operand register is capable of storing an address exceeding 16 bits; and

an execution unit for executing the decoded instruction.

63. (Amended) A data processor performing data processing based on an 8-bit instruction, comprising:

a plurality of registers;

a decoding unit decoding an 8-bit instruction, the instruction independently designating:

one of a plurality of operations including transfer and calculation;

one of the plurality of registers as a source operand, and

one of the plurality of registers as a destination operand;

wherein at least one instruction is further followed by a linear absolute address of more than 16 bits; and

an execution unit for executing the decoded instruction.

64. (Amended) A data processor performing data processing based on an 8-bit instruction, comprising:

a first register and a second register,

a decoding unit decoding an 8-bit instruction,

a judgment means for judging which one of sign-extending and zero-extending is to be performed on operand data is made depending on which of the first register and the second register is designated as the destination operand in the instruction, and

an execution unit for executing the decoded instruction.

65. (Amended) A data processor performing data processing based on an 8-bit instruction, comprising:

a plurality of registers;

a decoding unit for decoding an 8-bit instruction, the instruction independently designating:

one of a plurality of operations including transfer and calculation;

one of the plurality of registers as a source operand, and

one of the plurality of registers as a destination operand;

wherein an address register and a data register are included in the plurality of registers, and

an address stored in the address register is longer than data stored in the data register.

Please add the following new Claims 66-79:

66. The data processor of Claim 63, wherein the plurality of registers includes at least one register storing an address exceeding 16 bits.

67. The data processor of Claim 64, wherein the data processor performs data processing based on an 8-bit instruction, the instruction independently designating:

one of a plurality of operations including transfer and calculation;

one of the registers as a source operand, and

one of the registers as a destination operand.

68. A data processing method for performing data processing of an 8-bit instruction, comprising

decoding a first portion of the 8-bit instruction which independently designates one of a plurality of operations including transfer and calculation,

decoding a second portion of the 8-bit instruction which independently designates one of a plurality of registers as a source operand,

decoding a third portion of the 8-bit instruction which independently designates one of the plurality of registers as a destination operand,

wherein at least one of the source operand register and the destination operand register is capable of storing an address exceeding 16 bits; and

executing the instruction in accordance with the decoded results.

69. A data processing method for performing data processing of an 8-bit instruction, comprising

decoding a first portion of the 8-bit instruction which independently designates one of a plurality of operations including transfer and calculation,

decoding a second portion of the 8-bit instruction which independently designates one of a plurality of registers as a source operand,

decoding a third portion of the 8-bit instruction which independently designates one of the plurality of registers as a destination operand,

wherein the instruction is further followed by a linear absolute address exceeding 16 bits; and

executing the instruction in accordance with the decoded results.

70. The data processing method of Claim 69, wherein the plurality of registers includes at least one register storing an address exceeding 16 bits.

71. A data processing method for performing data processing of an instruction using a processor having a first register and a second register, comprising

judging which one of sign-extending and zero-extending is to be performed on operand data depending on which of the first register and the second register is designated as the destination operand in the instruction, and

performing one of sign-extending and zero-extending on operand data which is judged to be performed.

72. The data processing method of Claim 71, wherein the instruction is an 8-bit instruction which independently designates:

one of a plurality of operations including transfer and calculation;

one of a plurality of registers as a source operand, and

one of the plurality of registers as a destination operand;

the data processing method further comprising:

decoding a first portion of the 8-bit instruction which independently designates one of a plurality of operations including transfer and calculation,

decoding a second portion of the 8-bit instruction which independently designates one of a plurality of registers as a source operand, and

decoding a third portion of the 8-bit instruction which independently designates one of the plurality of registers as a destination operand, and

executing the instruction in accordance with the decoded results, including performing one of sign-extending and zero-extending which is judged to be performed.

73. A data processing method for performing data processing of an 8-bit instruction, comprising

decoding a first portion of the 8-bit instruction which independently designates one of a plurality of operations including transfer and calculation,

decoding a second portion of the 8-bit instruction which independently designates one of a plurality of registers as a source operand,

decoding a third portion of the 8-bit instruction which independently designates one of the plurality of registers as a destination operand,

wherein an address register and a data register are included in the plurality of registers, and an address stored in the address register is longer than data stored in the data register; and

executing the instruction in accordance with the decoded results.

74. A recording medium recording machine readable program instructions executed by a processor, the processor performing data processing of an 8-bit instruction comprising

a first portion which independently designates one of a plurality of operations including transfer and calculation,

a second portion which independently designates one of a plurality of registers as a source operand, and

a third portion of the 8-bit instruction which independently designates one of the plurality of registers as a destination operand,

wherein at least one of the source operand register and the destination operand register is capable of storing an address exceeding 16 bits.

75. A recording medium recording machine readable program instructions executed by a processor, the processor performing data processing of an 8-bit instruction comprising

a first portion which independently designates one of a plurality of operations including transfer and calculation,

a second portion which independently designates one of a plurality of registers as a source operand, and

a third portion of the 8-bit instruction which independently designates one of the plurality of registers as a destination operand,

wherein the instruction is further followed by a linear absolute address exceeding 16 bits.

76. The recording medium of Claim 75, wherein the plurality of registers includes at least one register storing an address exceeding 16 bits.

77. A recording medium recording machine readable program instructions executed by a processor, the processor performing data processing of an 8-bit instruction, the 8-bit instruction comprising:

a designation of one of a first register and a second register as containing a destination operand for the instruction,

wherein a judgment of which one of sign-extending and zero-extending is to be performed on operand data is made depending on which of the first register and the second register is designated as the destination operand in the instruction.

78. The recording medium of Claim 77, wherein the 8-bit instruction further comprises:

a first portion which independently designates one of a plurality of operations including transfer and calculation,

a second portion which independently designates one of a plurality of registers as a source operand, and

a third portion of the 8-bit instruction which independently designates one of the plurality of registers as a destination operand,

wherein the first register and the second register are included in the plurality of registers.

79. A recording medium recording machine readable program instructions executed by a processor, the processor having a plurality of registers, the processor performing data processing of an 8-bit instruction comprising:

a first portion which independently designates one of a plurality of operations including transfer and calculation,

a second portion which independently designates one of a plurality of registers as a source operand, and

a third portion of the 8-bit instruction which independently designates one of the plurality of registers as a destination operand,

wherein an address register and a data register are included in the plurality of registers, and an address stored in the address register is longer than data stored in the data register.